

CLAIMS

What is claimed is:

1. A method for recovering from data errors within a processor, comprising the steps of:

5 storing a backup of data for a register of a register file and within a buffer;
periodically checking for data errors within the processor; and
restoring the data from the buffer to the register file in the event of data errors.

10 2. A method of claim 1, the step of restoring comprising restoring data from the buffer over a prior period before checking for data errors.

3. A method of claim 1, further comprising loading new data to the register and after the step of storing.

4. A method of claim 1, further comprising loading new data to the register and concurrently with the step of storing.

15 5. A method of claim 1, the step of storing the data within the buffer comprising storing the data within a second register file.

6. A method of claim 1, further comprising the step of flushing the buffer after checking for, and detecting no, data errors.

20 7. A method of claim 1, further comprising the step of freezing execution of instructions within pipelines of the processor after detecting data errors.

8. A method of claim 1, further comprising the step of backing up a program counter of the processor after detecting errors.

25 9. A method of claim 8, further comprising the step of re-executing a program through the processor at a time associated with the backed up program counter.

10. A method of claim 1, the step of periodically checking for data errors comprising periodically checking for the data errors at sequential time periods defined by a number of processor clock cycles.

11. A method of claim 1, further comprising the steps of utilizing an error correction code in connection with data storage to the buffer.
12. A processor with register file data recovery, comprising:
an execution unit having a plurality of pipelines for processing program
instructions relative to a program counter;
a register file, wherein one or more stages of the pipelines loads data to a
register of the register file; and
a buffer for storing a backup of data within the register and for restoring data
to the register file in the event of data errors within the processor.
13. A processor of claim 12, the buffer comprising a second register file.
14. A processor of claim 12, the register file comprising an extra read port
for reading the data from the register.
15. A processor of claim 12, the register file comprising a write port for
writing the data from the buffer to the register.
16. A processor of claim 12, further comprising one or more error detectors
for detecting the data errors.
17. A processor of claim 16, the error detectors comprising redundant logic
devices.
18. A processor of claim 12, further comprising error correction code for
data recovery of data stored within the buffer.
19. A processor of claim 12, the buffer reading data within the register
prior to an execution stage for an instruction identifying a write to the register.
20. A processor of claim 12, further comprising a program counter, the
program counter being reset in connection the buffer restoring data to the register file.